

U.S. Appln. No. 09/901,273  
Reply to Office Action dated June 10, 2005

PATENT  
450117-03383

**IN THE CLAIMS**

1. (Currently Amended) An I/Q demodulator comprising:  
an n-port structure being supplied with a first RF signal to be demodulated at a  
first input and with a second RF signal to be demodulated at a second input, said n-port structure  
outputting n-2 output signals of a plurality of power sensors, with n being 4, 5 or 6, and

a multiplexing means for multiplexing low-pass-filtered output signals of the  
plurality of power sensors to a single output.

2. (Previously Presented) The I/Q demodulator according to claim 1,  
wherein said I/Q demodulator further comprises a single A/D converter that is supplied with an  
analog signal originating from the multiplexing means and outputting a digitally converted signal  
to a digital processing unit.

3. (Previously Presented) The I/Q demodulator according to claim 2,  
wherein the A/D converter has an adaptive sampling rate.

4. (Previously Presented) The I/Q demodulator according to claim 2,  
wherein the digital processing unit comprises an adaptive baseband filtering unit.

5. (Previously Presented) The I/Q demodulator according to claim 1,  
wherein the output signals of the plurality of power sensors are selectively passed through  
different low-pass-filters having different cut-off-frequencies.

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6. (Previously Presented) The I/Q demodulator according to claim 5, wherein said I/Q demodulator further comprises switches for selecting the different low-pass-filters.

7. (Previously Presented) The I/Q demodulator according to claim 1, wherein the n-port structure is a five-port-junction.

8. (Previously Presented) The I/Q demodulator according to claim 1, wherein the n-port structure is a four-port-junction and the demodulator is a (M)QAM or a (M)PSK demodulator.

9. (Previously Presented) The I/Q demodulator according to claim 1, wherein the multiplexing means is a DC-switch with a switching time of  $\frac{1}{n-2}$  times a symbol duration.

10. (Previously Presented) The I/Q demodulator according to claim 1, wherein before or after the multiplexing means at least one DC-amplifier is provided.

11. (Previously Presented) The I/Q demodulator according to claim 1, further comprising a low-pass-filter following the multiplexing means and, said low-pass filter having a cut-off-frequency of  $\frac{n-2}{2} B$ , whereby the output signals of the plurality of power sensors are low-pass-filtered with a cut-off-frequency of  $\frac{B}{2}$ , where B is a maximum bandwidth of the RF signal to be demodulated.

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12. (Previously Presented) The I/Q demodulator according to claim 1, wherein the n-port structure, the plurality of power sensors and said multiplexing means are integrated on a single chip.

13. (Previously Presented) A software radio device wherein said radio device comprises an I/Q-demodulator according to claim 1.

14. (Currently Amended) A method for I/Q-demodulation, said method comprising the steps of:

inputting a first RF signal to be demodulated in an n-port structure,  
inputting a second RF signal in an n-port structure,  
detecting the power of n-2 output signals of a plurality of output sensors of the n-port structure, n being 4, 5 or 6,  
low-pass-filtering the detected power signals, and  
multiplexing the low-pass-filtered power signals to a single output.

15. (Previously Presented) The method according to claim 14, said method further comprising the step of:

supplying a single A/D converter with the multiplexed power signals and  
outputting a digitally converted signal to a digital processing unit.

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16. (Previously Presented) The method according to claim 15, said method further comprising the step of:

adapting a sampling rate of the A/D converter depending on a bandwidth of the RF signal to be demodulated.

17. (Previously Presented) The method according to claim 14, wherein the power signals are selectively filtered with different cut-off-frequencies.

18. (Previously Presented) The method according to claim 14, wherein the step of multiplexing is implemented by a DC-switch with a switching time  $\frac{1}{n-2}$  of a symbol duration.

19. (Previously Presented) The method according to claim 14, wherein the multiplexed power signals are low-pass-filtered with a cut-off-frequency of  $\frac{n-2}{2} B$ , whereby non-multiplexed power signals are low-pass-filtered with the a cut-off-frequency of  $\frac{B}{2} \}$ , where  $B$  is a maximum bandwidth of the RF signal to be demodulated.